DDR3 SDRAM SEE TEST REPORT

I. Introduction

This report describes the SEE testing and characterization carried out for the Samsung K4B1G0846DHCF8 1G DDR3 SDRAM for NEPP (NASA Electronic Parts and Packaging Program). The goals of the testing are to elucidate the heavy-ion and proton-induced single-event-effect modes that could affect performance of the part in space radiation environments. Because the part is a DDR SDRAM, sampling is done on both the rising and falling clock edges in normal operation. This gives rise to an effective operating speed of ~1 GHz for an input clock speed of 500 MHz. Such speeds are significantly higher than those of most components used in spaceflight data operations. However, it is also possible to run the memory at lower speed with the PLL disabled. Although it is highly desirable to perform testing both with PLL enabled and disabled, the speeds required precluded enabling the PLL for this test. We operated the DDR3 with the latest High-Speed Digital Tester HSDT) while irradiating it with protons at the Indiana University Cyclotron Facility (IUCF) and heavy ions at the Texas A&M University Cyclotron Facility (TAMU).

II. Device Description

The Samsung K4B1G0846DHCF8 is a 1 Gbit third generation DDR (DDR3) SDRAM fabricated by Samsung in their 65 nm CMOS process. Device input/output is organized in a 128M×8 configuration, with 8 banks. Device operation is described in the DDR3 SDRAM Specification (June 2007). With the PLL enabled, data can be written or read on both the rising and falling edges of the clock, effectively doubling device speed. However, with PLL disabled, operating frequencies are limited to speeds below 20-100 MHz. BGA package mounting is shown in figure 1.

Table I. Device information

Mfg. and Part Number	Samsumg K4B1G0846DHCF8
Manufacturer:	Samsung
Lot Date Code (LDC):	
Quantity Tested:	3
Serial Numbers of Control Sample:	1
Serial Numbers of Radiation Samples:	2, 3, 4, 5, 6
Part Function:	DDR3 SDRAM
Part Technology:	65 nm CMOS
Package Style:	72 pin FBGA, thinned
Test Equipment:	Power Supply, HSDT, multimeters
Test Engineer:	H. Kim, M. Friendlich

3.2 x8 Package Pinout (Top view) : 82ball FBGA Package(78balls + 4 balls of support balls)

	1	2	3	4	5	6	7	8	9	10	11	
A	NC	V_{SS}	V_{DD}	NC				NU/$\overline{TDQS}$	V_{SS}	V_{DD}	NC	A
B		V_{SS}	V_{SSQ}	DQ0				DM/TDQS	V_{SSQ}	V_{DDQ}		B
C		V_{DDQ}	DQ2	DQS				DQ1	DQ3	V_{SSQ}		C
D		V_{SSQ}	DQ6	$\overline{DQS}$				V_{DD}	V_{SS}	V_{SSQ}		D
E		V_{REFDQ}	V_{DDQ}	DQ4				DQ7	DQ5	V_{DDQ}		E
F		NC	V_{SS}	$\overline{RAS}$				CK	V_{SS}	NC		F
G		ODT	V_{DD}	$\overline{CAS}$				$\overline{CK}$	V_{DD}	CKE		G
H		NC	$\overline{CS}$	$\overline{WE}$				A10/AP	ZQ	NC		H
J		V_{SS}	BA0	BA2				NC	V_{REFCA}	V_{SS}		J
K		V_{DD}	A3	A0				A12/$\overline{BC}$	BA1	V_{DD}		K
L		V_{SS}	A5	A2				A1	A4	V_{SS}		L
M		V_{DD}	A7	A9				A11	A6	V_{DD}		M
N	NC	V_{SS}	$\overline{RESET}$	A13				NC	A8	V_{SS}	NC	N

Note : Green NC balls (A1, A11, N1 and N11) indicate mechanical support balls with no internal connection.

Ball Locations (x8)

● Populated ball
\+ Ball not populated

Top view
(See the balls through the package)

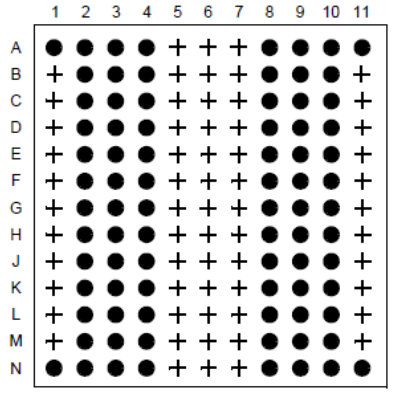


Figure 1 BGA package for the DDR3.

III. Test Conditions

Test Temperature: Room Temperature
Operating Frequency: <100 MHz (PLL disabled)
Power Supply Voltage: biased at 1.8V.
Device Operating Mode: Self-refresh
Test Modes: Read-Correct-Write, Double-Read, Read-Write-Change Pattern-Read-Write
Test Patterns: All-0's, All-1's, AA, 55, checkerboard + inverse, marching 1's (?)

IV. Test Method

Proton testing will be done at the Indiana University Cyclotron Facility (IUCF). The test parts will be unthinned, packaged parts mounted onto daughter cards for the GSFC HSDT. Table I gives ions likely to be used in the test:

Table II: Test Ions at IUCF

Ion	**Energy (MeV)**
H+	89-198

Table III: Test Ions at TAMU

Ion-Energy (MeV)	LET-@ active area (MeVcm2/mg)	Range from surface (μm)
Ne-545	2.3	799
Ar-991	7.8	499
Kr-2081	28.8	332
Xe-3197	55.3	286

We slated 3 samples for proton testing and 3 for heavy-ion testing. Proton testing does not require modification of the Flip-chip ball-grid array package for these parts, so all 3 samples were functional. On the other hand, only one sample for heavy-ion testing survived thinning and transport. For proton testing, we anticipated that total dose effects could limit the number of runs taken with a single sample. However, based on previous generations, we concluded that the parts were likely hard to ~100-200 krad(Si). The main goal of both tests was to determine the susceptibility of the SDRAMs to SEU, control logic errors (including SEFI) and stuck bits. Although SEL was deemed unlikely for protons, the same power-control system was used for proton and heavy-ion testing, so for both tests we limited the current to the DUT to levels just above the normal operational level.

In the lab at GSFC: The parts were characterized at various operating speeds and for all test patterns (all zeros, all ones, checkerboard, etc.) to determine the operational conditions feasible for testing using the HSDT. One important goal of this testing was to determine the maximum current likely to occur during normal operation.

For the parts slated for heavy-ion testing, there were additional concerns, including the need to thin the parts so the ion beam could penetrate to the sensitive volume and the risk that strain on the thinned die could cause failure of parts over time. For this reason, we tried to keep mounting and demounting of the daughter card to a minimum once functionality had been verified.

At IUCF: The devices were tested for functionality both in the control room and in the beam line. Once mounted with the DUT in the beam path, the DUT was written with a selected pattern and the pattern was verified. The tester then cycled through the memory continually, reading each memory location and comparing the contents to the expected values. If a discrepancy was noted, the error was recorded and

the contents of the address were corrected with the expected pattern. If a large block error was observed, irradiation was stopped while it was determined whether the device would recover. If no recovery was seen in a reasonable time (e.g. 30 seconds), various recovery strategies were carried out, beginning with refreshing mode registers, then DUT soft reset, DUT hard reset and finally power cycling the DUT. If the block error involved a high current, but did not automatically trip the current limit for power to the device, the error mode was considered a SEL/microlatch.

The placement of the FPGA and the voltage reference limited the angles at which data could be taken in both the tilt and roll directions. Even with the beam incident normally on the DUT, we had to shield the voltage reference and FPGA to limit neutron-induced errors in these devices (see figure 2). Lightning strikes that disabled portions of the accelerator limited testing to about half the allotted time of 8 hours. As such most of the testing was conducted at a beam energy of 198 MeV, although a few runs were carried out for 89.8 MeV protons.

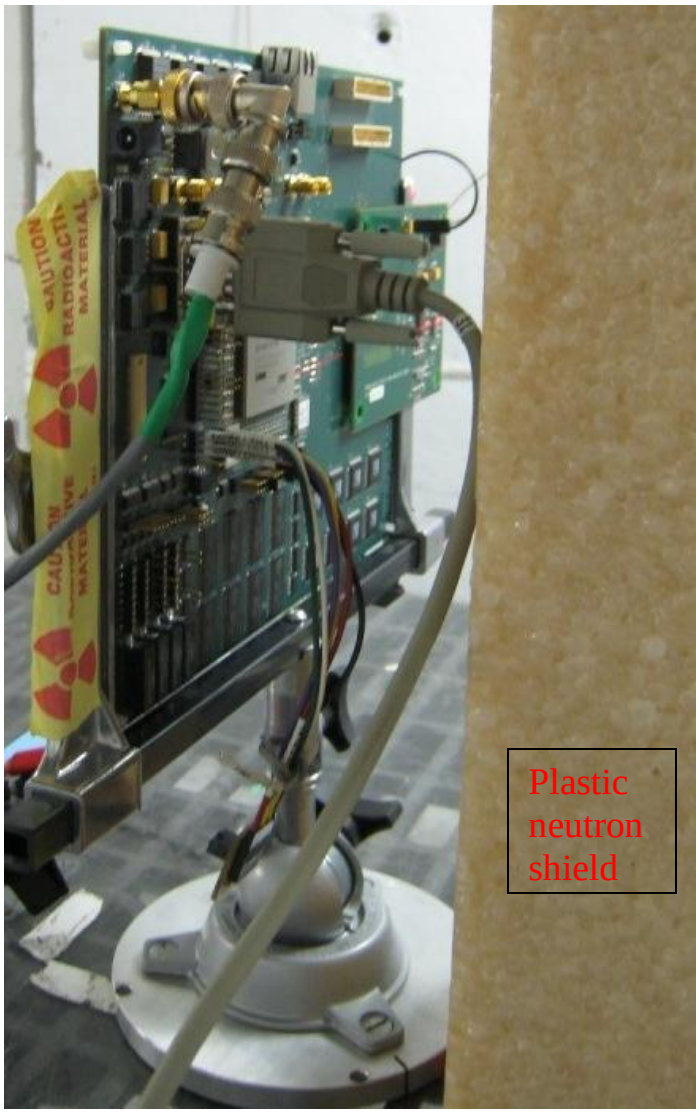
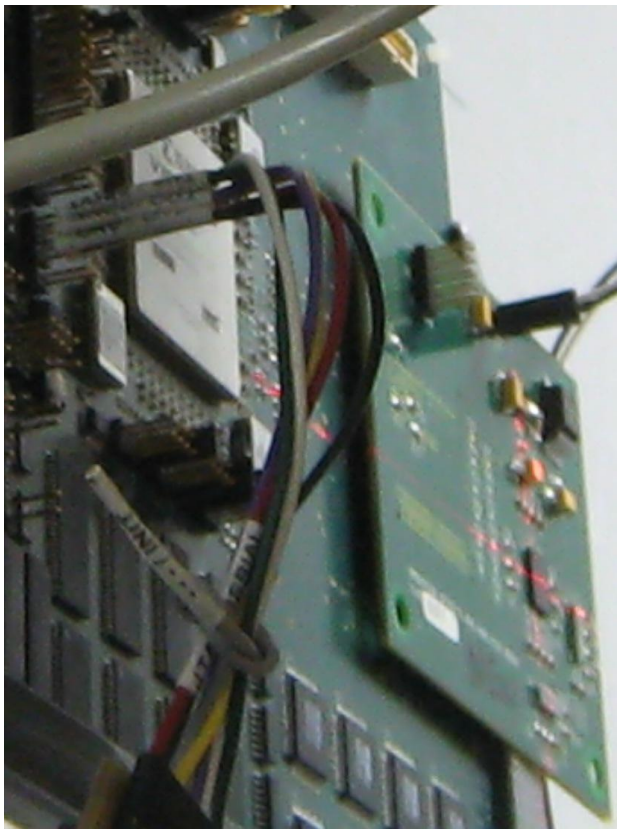


Figure 2 DDR3 centered in the baeam-line laser cross hairs at IUCF. The plastic block at the right of the figure is needed to shield the voltage reference and FPGA from secondary neutrons. The photo below shows a closeup of the part in the cross-hairs.



At TAMU: Parts were verified functional using several different test patterns to ensure there had been no failures in transit. Only one of the parts was still operational. The other seemed to be giving errors in its address lines and could not be used. The remaining part was verified to be fully functional and then placed in line with the ion beam. A test pattern was written and verified. Testing then followed the same procedure as for the proton test at IUCF.

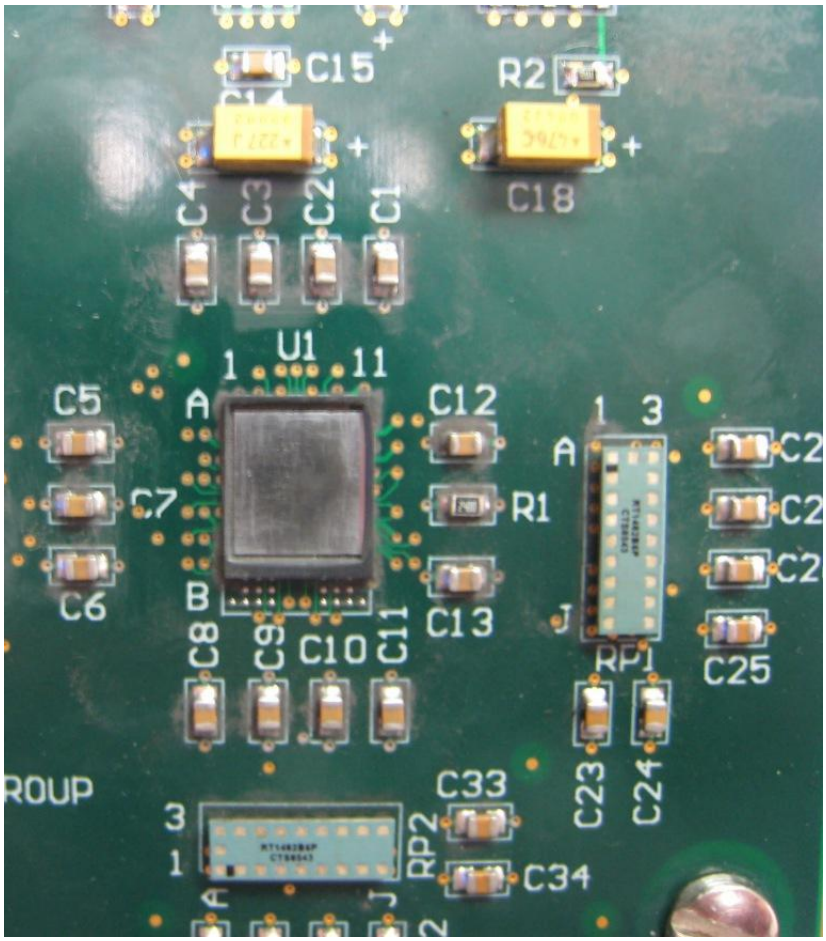


Figure 3 The thinned DDR3 SDRAM is shown (gray, center labeled U1) on the test board prior to heavy-ion testing at TAMU.

V. Results

Despite the limited beam time and limited ability to take angular exposures, we carried out irradiation for several data patterns and at two different energies. Angular exposures tended to result in hits to the tester or voltage reference that rendered the data unreliable. Unlike previous DDR parts, error cross sections for the Samsung DDR3 parts exhibited significant pattern dependence, with upsets much more likely going from 1-to-0 rather than 0-to-1. This was evident in both proton testing (Figure 4) and heavy-ion testing (Figures 5 and 6.)

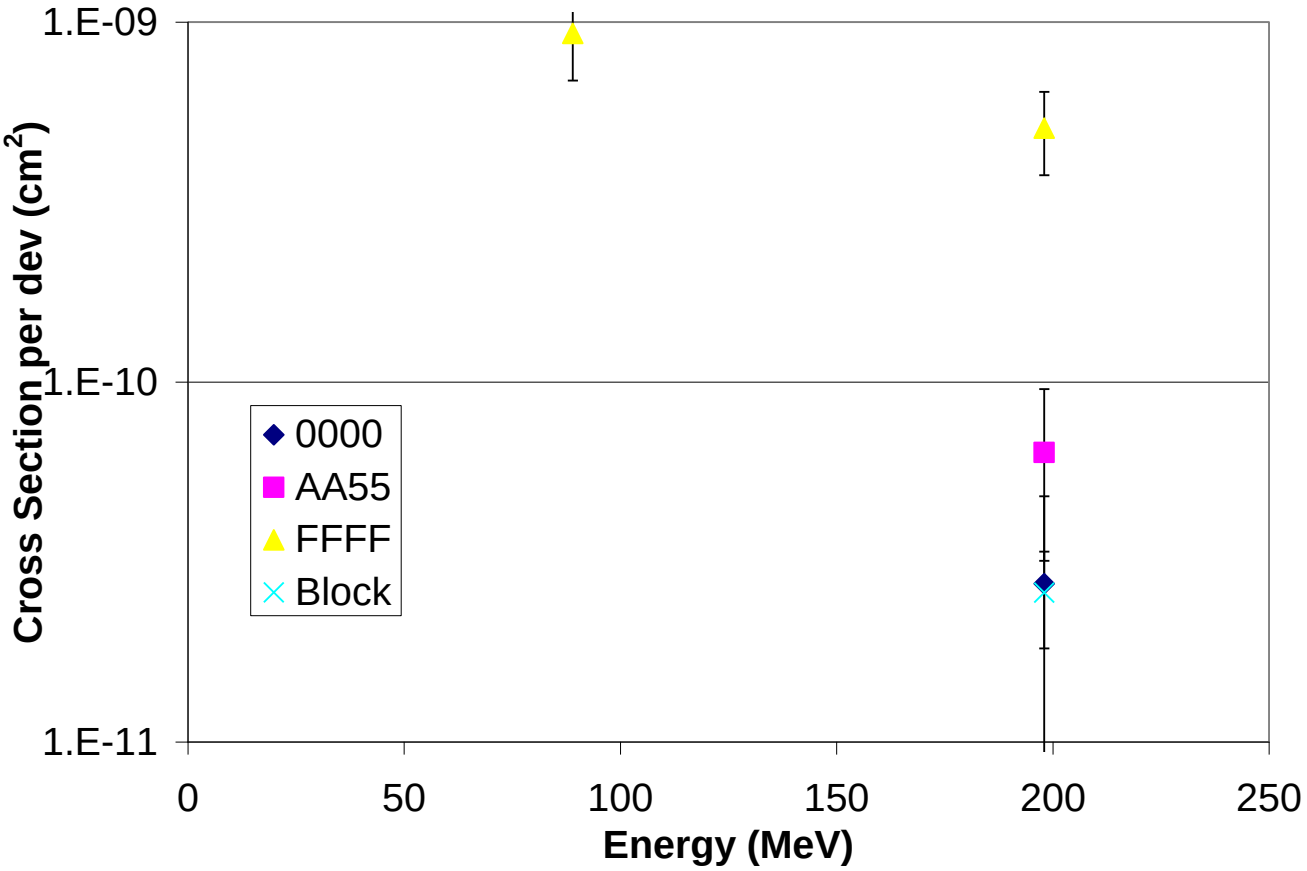


Figure 4 Cross sections for proton induced SEU as a function of proton energy and data pattern. No significant energy dependence is seen over the range of proton energies. However, there is a strong dependence on data pattern.

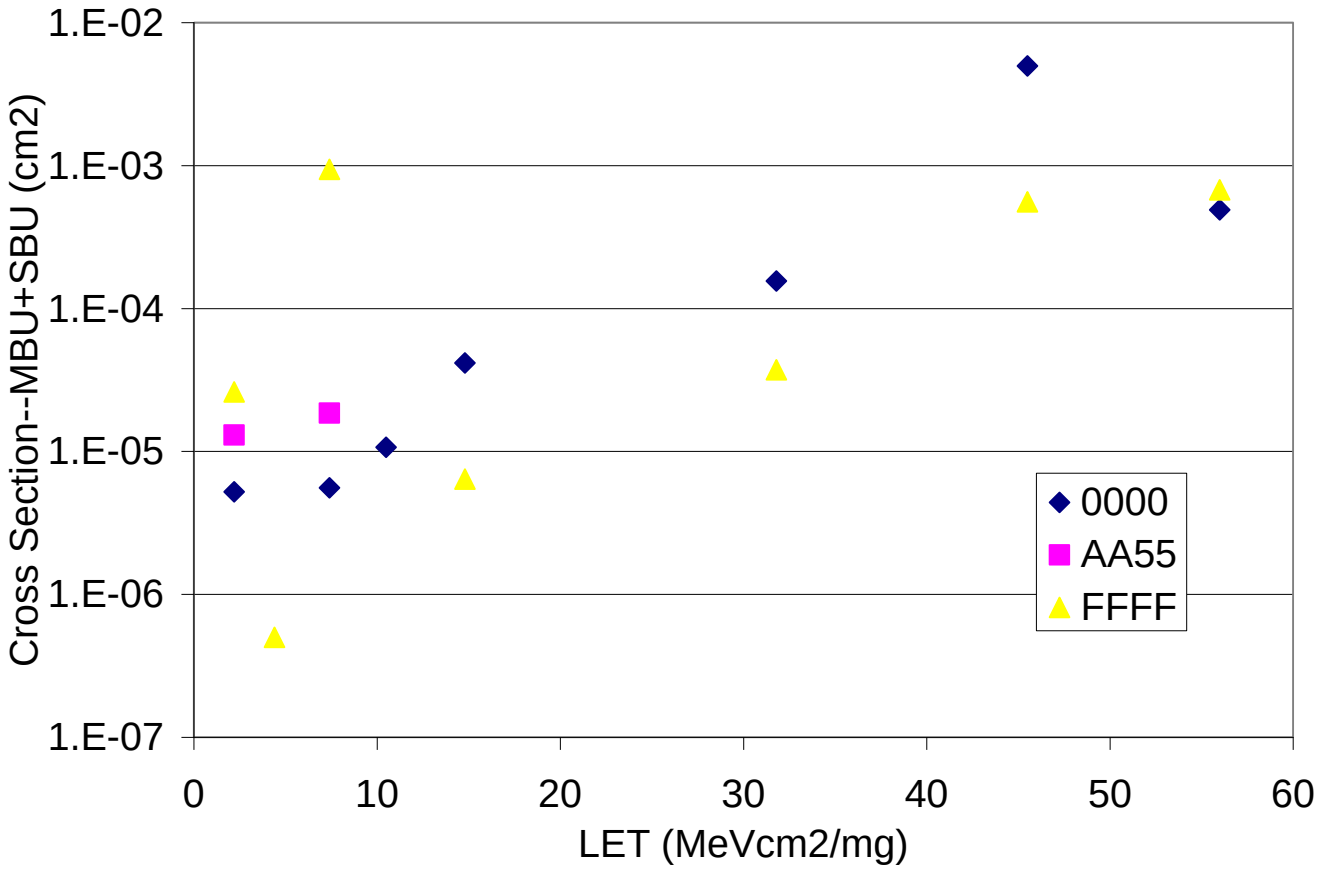


Figure 5 SEU cross section vs. LET for various data patterns. Upsets from 1 to 0 are much more likely than from 0 to 1, and the cross section does not scale with effective LET at low LET values.

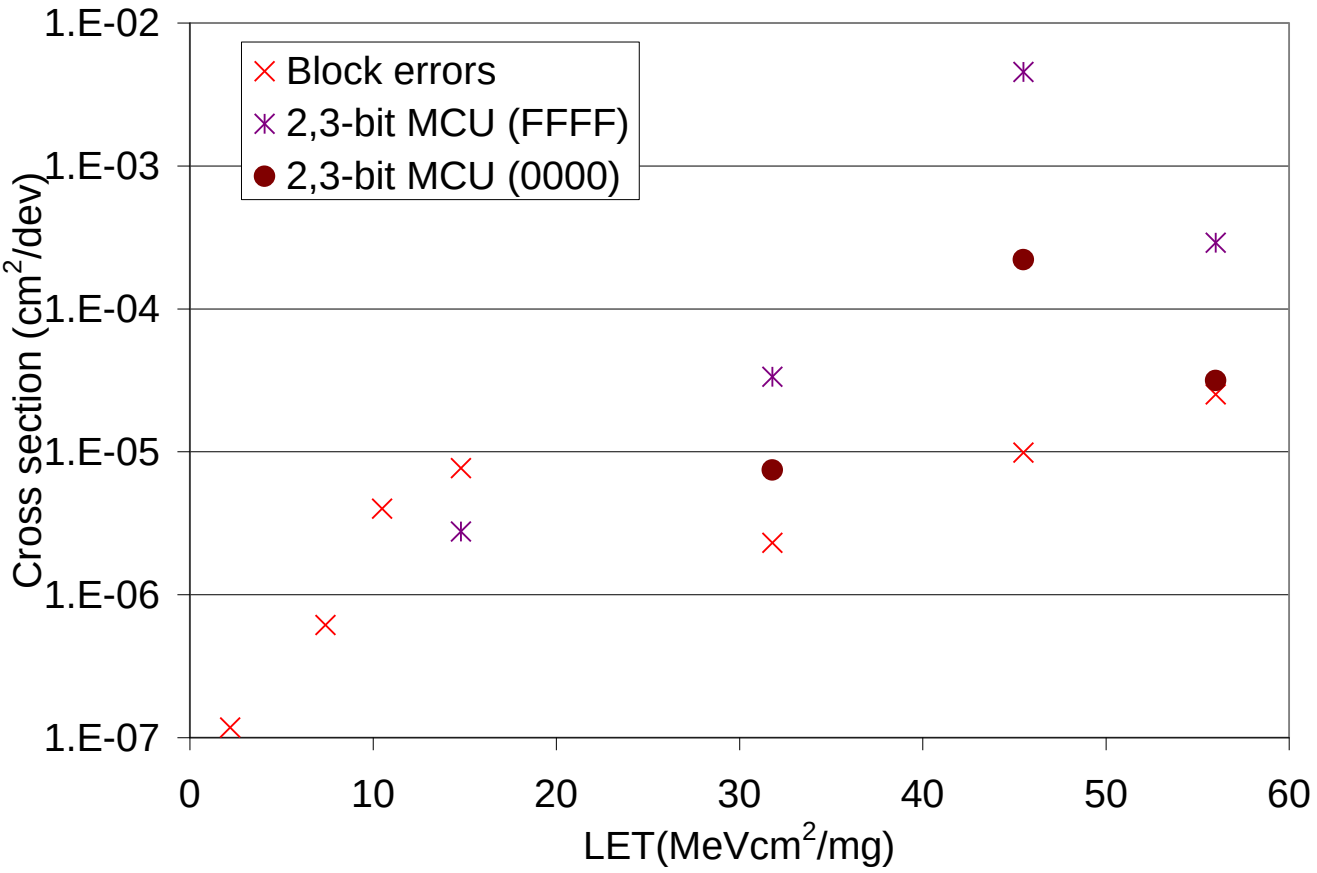


Figure 6 Cross section for block errors and multicell upsets (for two data patterns) as a function of LET. All three error modes seem to follow effective LET.

The most notable aspects of the SEU plot are the lack of effective LET scaling at low LET and the asymmetry for 1→0 and 0→1 errors. This asymmetry was not evident for DDR and DDR2 tests—although this is the first test we have performed with the PLL disabled.
In this work, we have identified block errors by their proximity in time and or addresses. It may be that the parts experienced some sort of logic error that was not detectable using either time of error or address information, and this could have yielded the anomalously high data point for Ar at 0 degrees.. We note that 3 separate runs for this ion and angle performed very similarly.
In post processing, we observed a significant number of errors with nearly simultaneous times of occurrence and column numbers differing by 8. It is likely that these events represent a single multi-cell error and that the bits of the DDR3 are interleaved with physically adjacent cells being 8 columns apart logically. We have included each incidence as a single error in the SEU plot and plotted separate multi-cell upset cross sections along with block errors in figure 5.

SEFI events were seen only for high-fluence runs at high LET. These runs also showed high-current events, although the current always recovered spontaneously, indicating that the high current was likely due to bus contention. Finally, we note that after the last run, we noticed 3

bits that tended to read in error, suggesting that they were “stuck” or at least leaky. The device received about 110 krad(Si) of heavy-ion dose. The maximum dose during proton testing for any part was ~60 krad(Si) of proton dose.

VI. Conclusion

Due to the inability of the HSDT to accommodate the full speed of the DDR3, the Samsung parts were tested with the PLL disabled. This led to the signals being somewhat noisy and the need to operate the parts at only 25 MHz.

The current tests yielded results somewhat different from what was observed in the Samsung DDR2 test. The SEU limiting cross section was about an order of magnitude lower, and exhibited more asymmetry between $1\rightarrow0$ and $0\rightarrow1$ errors. At present, we cannot say whether this is due to architectural differences between DDR2 and DDR3 or whether the lack of errors due to the PLL allowed us more easily to pick out such trends. In addition, we saw stuck bits for the DDR3 under heavy-ion irradiation, and this susceptibility was not evident in previous tests.

Because of the unresolved questions about whether these differences arise from the lack of PLL or from differences from DDR2 to DDR3, it would be desirable to test the DDR3 with PLL enabled and to carry out a TPA laser test. These tests should be carried out before these parts are considered for space applications.